40Pin Flash Disk Module Min.16MB ~ Max.512MB,
True IDE Interface

1. PRODUCT OVERVIEW

GENERAL DESCRIPTION

The HFDOM40S3Rxxx series 40Pin Flash Disk Module is a flash technology based with True IDE interface flash memory card. It is constructed with flash disk controller chip and NAND-type (Samsung) flash memory device. The HFDOM40S3R-xxx series operates in both 3.3-Volt and 5.0-Volt power supplies. It comes in capacity of 16, 32, 48, 64, 80, 96, 128, 144, 160, 192, 208, 224, 256, 272,288, 320, 384 and up to 512MByte formatted 40Pin type .

By optimizing flash memory management, the life of this HFDOM40S3Rxxx series can be extended to its maximum level. Because the ECC function is included, the correctness of data transfer between the HFDOM40S3Rxxx series and a True IDE compatible interface device can be guaranteed.

The HFDOM40S3Rxxx series is fully compatible with applications such as CPU card / board, set top box, industry / military PC / Notebook, security equipment, measuring instrument and embedded systems.

FEATURES

- ATA / True IDE compatible host interface
- ATA command set compatible
- Automatic sensing of PC Card ATA or true IDE host interface.
- Very high performance, very low power consumption
- Automatic error correction
- Auto Standby to save power consumption.
- Supports power down commands and sleep modes.
- Integrated PCMCIA attribute memory of 256 bytes (CIS)
- Support for 8 or 16 bit host transfers
- 3.3V/5.0V operation voltage
- Host Interface bus width : 8/16 bit Access
- Flash Interface bus width : 8 bit Access
- Capacity : Min. 16MB ~ Max. 512MB
- MTBF > 1,000,000 hours.
- Minimum 10,000 insertions.
- Shock : 2,000 G max.
- Vibration : 15 G peak to peak max.

PRODUCT SPECIFICATIONS

Capacities :

16, 32, 48, 64, 80, 96, 128, 144, 160, 192, 208, 224, 256, 272,288, 320, 384 and up to 512MB (formatted)

System Compatibility :

Please refer to the compatibility list of index.

Performance :

Host Data Transfer Rates : up to 16.6 MB/sec, PIO mode 4; 16.6MB/sec

Operating Voltage : 3.3V / 5.0V ±10%

Power consumption : 3.3V ± 5%

Read mode	<30 mA
Write mode	<56 mA
Stop mode	<2 mA

Environment conditions :

Operating temperature	0°C to + 70°C
Storage temperature	- °C to + °C
Relative humidity	8% to 95%, non-condensing

ELECTRICAL SPECIFICATIONS

Table 1.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DD}	Power supply	-0.3 to 6.0	V
V_{IN}	Input voltage	-0.3 to V_{DD}+0.3	V
V_{OUT}	Output voltage	-0.3 to V_{DD}+0.3	V
T_{STG}	Storage temperature	−55 to 150	^{o}C

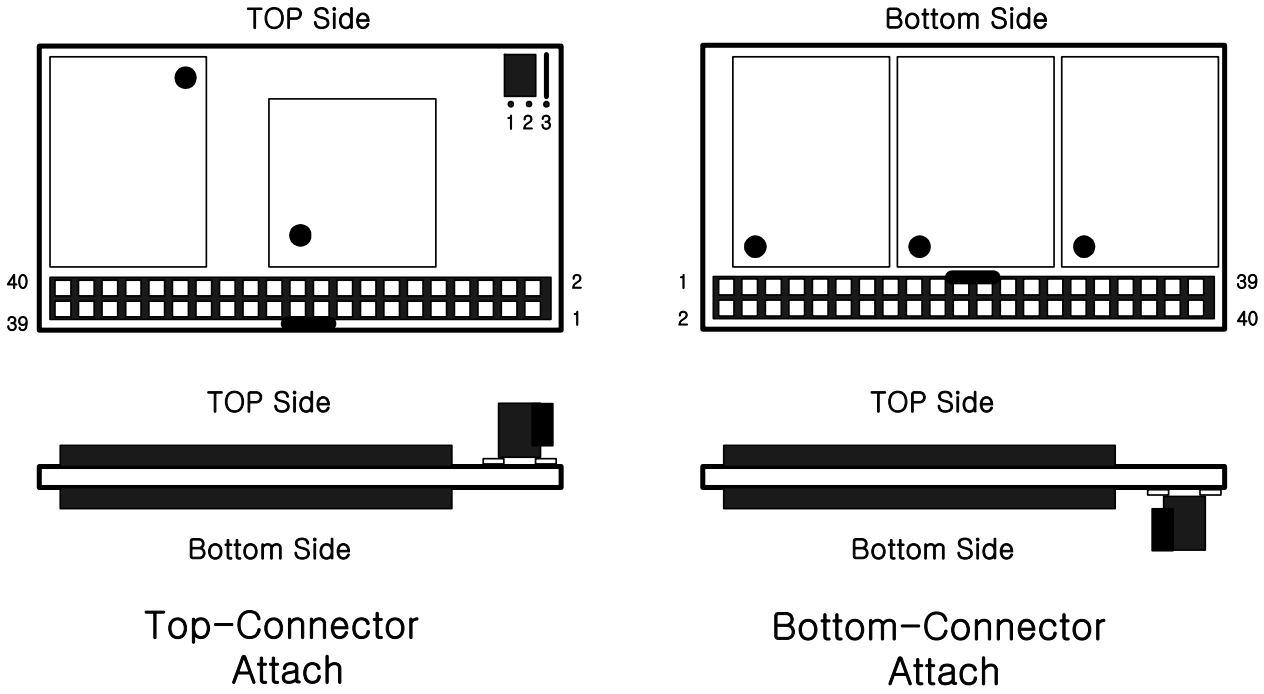
Table 1.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Power supply	3.0	3.6	V
V_{IN}	Input voltage	-0.3	V_{DD}+0.3	V
T_{OPR}	Operating temperature	0	70	^{o}C

Table 1.3 DC Characteristics

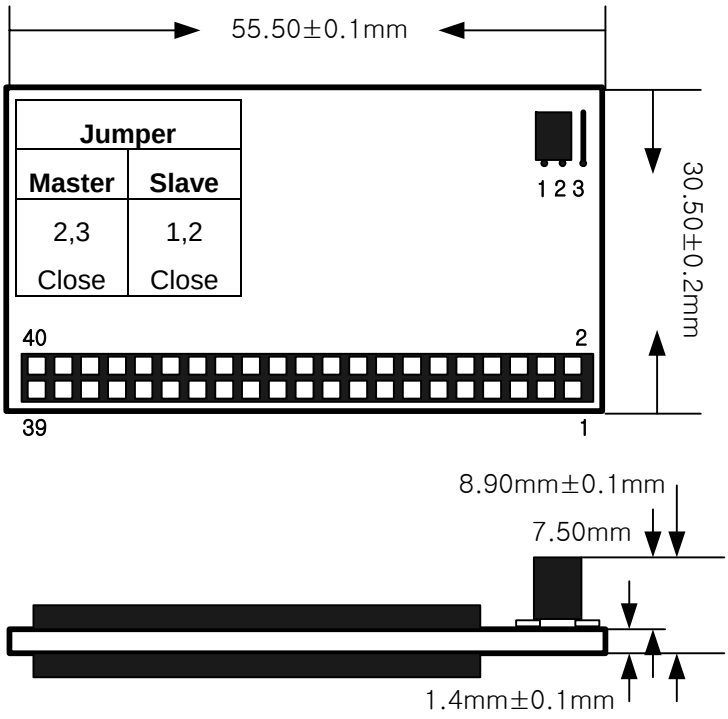
Sym.	Parameter	Min	Typ	Max	Units
V_{IL}	Input low voltage			$0.3V_{DD}$	V
V_{IH}	Input high voltage	$0.7V_{DD}$			V
V_{IL}	Schmitt input low voltage		1.22		V
V_{IH}	Schmitt input high voltage		2.08		V
V_{OL}	Output low voltage			0.4	V
V_{OH}	Output high voltage	2.3		1	V
R_I	Input pull up/down resistance		75		kΩ

PHYSYCAL SPECIFICATION



Top-Connector Attach

Bottom-Connector Attach



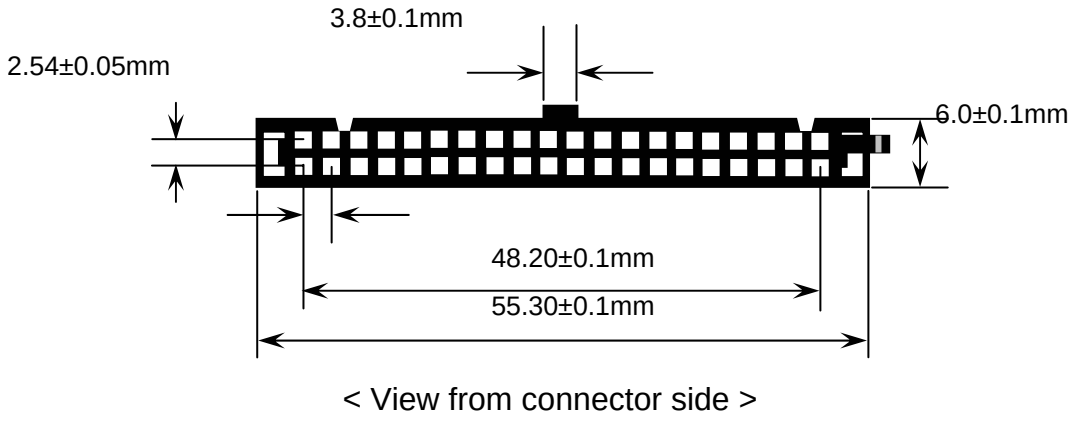


Figure 1.0 40 pin Type Flash Disk Module Dimensions

INSTALLTION GUIDE

1) Setting Method

① Make sure your computer is turned off before you open the case.

② Plug the carefully into the 40pin IDE slot on your computer.
Caution: Make sure to align pin1 on host adapter interface connector with pin 1 on your Flash Disk Module. Pin 1 is indicated by a triangle on the Flash Disk Module connector.

③ The Flash Disk Module is used power connector cable of the computer.
Caution: If you need to remove your Flash Disk Module, use both hands to pull it out carefully.

④ Check all cable connections and then replace your computer cover.

2) BIOS setting Method

Before you format or partition your new drive, you must configure your computer's BIOS so that the computer can recognize your new drive.

① Turn your computer on. As your computer start up, watch the screen for a message describing how to run the system setup program on the screen (sometimes called BIOS or CMOS setup). This is usually done by pressing a special key, such as **Delete**, **Esc** or **F1** during startup. See your computer manual for details. Press the appropriate key to run the system setup program.

② ***If your BIOS provides automatic drive detection (an "AUTO" drive type), select this option.*** (**We recommend to use Normal / CHS mode to partition your Flash Disk Module to get the maximum formatted capacity.**)
This allows your computer to configure itself automatically for your new drive.
If your BIOS dose not provide "AUTO" drive detection, select "User-defined" drive setting and enter the CHS values from the table. BIOS Settings (see specification) Capacity Cylinders Heads Sectors(unformatted)

③ Save the settings and exit the System Setup program. (your computer will automatically reboot) After you configure your computer, you can use the standard DOS commands to partition and format your Flash Disk Module, as described below.

3) Formatting Method

To partition your new Flash Disk Module with Microsoft DOS program :

① Insert a bootable DOS diskette into your diskette drive and restart your computer.

② Insert a DOS program diskette that contains the **FDISK.EXE** and **FORMAT.COM** programs into your diskette drive. Use the same DOS version that is on your bootable diskette. At the **A:\ >** prompt, type **"FDISK"** and press **Enter**.

③ Select **"Create DOS partition or logical DOS drive"** by pressing **1**. Then press **Enter**.

④ Select **"Create primary DOS partition"** by pressing **1** again. Then press **Enter**.
Create your first drive partition. If you are creating a partition that will be used to boot your computer (drive C), make sure that the partition is marked active.

⑤ Create an extended partition and additional logical drives as necessary, until all the space on your new hard drive has been partitioned.

⑥ When the partitioning is complete, **FDISK** reboots your computer.
Caution: Make sure to use the correct drive letters so that you do not format a drive that already contains data.

⑦ At the **A:\ >** prompt, type **"format c:/s"**, where **c** is the letter of your first new partition, Repeat the format process for all the new partitions you have created.

⑧ After you format your drive, it is ready to use.

2. PIN INFORMATION

PIN ASSIGNMENTS AND PIN TYPE

Table 2.1 Pin Assignment and Pin type

Pin	Signal	Pin Type	Pin	Signal	Pin Type
1	/RESET	I	**2**	GND	Ground
3	D07	I/O	**4**	D08	I/O
5	D06	I/O	**6**	D09	I/O
7	D05	I/O	**8**	D10	I/O
9	D04	I/O	**10**	D11	I/O
11	D03	I/O	**12**	D12	I/O
13	D02	I/O	**14**	D13	I/O
15	D01	I/O	**16**	D14	I/O
17	D00	I/O	**18**	D15	I/O
19	GND	DC	**20**	Key Pin	--
21	INPACK	--	**22**	GND	Ground
23	/IOW	I	**24**	GND	Ground
25	/IOR	I	**26**	GND	Ground
27	IORDY	O	**28**	Reserved	--
29	REG	--	**30**	GND	Ground
31	IRQ	O	**32**	/IOIS16	O
33	A01	I	**34**	/PDIAG	I/O
35	A00	I	**36**	A02	I
37	/CS0	I	**38**	/CS1	I
39	/DASP	I/O	**40**	GND	Ground

Signal Descriptions

Table 2.2 Signal Descriptions

Signal Name	Dir.	Pin	Description
A[2:0]	I	33,35,36	In True IDE Mode only A[2:0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.
-PDIAG	I/O	34	This input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol.
-DASP	I/O	39	In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CS0, -CS1	I	37,38	CS0 is the chip select for the task file registers while CS2 is used to select the Alternate Status Register and the Device Control Register.
D[15:00]	I/O	3,4,5,6, 7,8,9,10, 11,12,13, 14,15,16, 17,18	All Task File operations occur in byte mode on the low order bus D00-D07 while all data transfers are 16 bit using D00-D15.
GND	--	2,19,22, 24,26, 30,40,	Ground.
-IOR	I	25	This is an I/O Read strobe generated by the host.
-IOW	I	23	The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the Storage Card controller registers when the Storage Card is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (trailing edge).
IRQ	O	31	In True IDE Mode signal is the active high Interrupt Request to the host.
-RESET	I	1	This input pin is the active low hardware reset from the host.
IORDY	O	27	This output signal may be used as IORDY.
-IOIS16	O	32	This output signal is asserted low when this device is expecting a word data transfer cycle.

BLOCK DIAGRAM

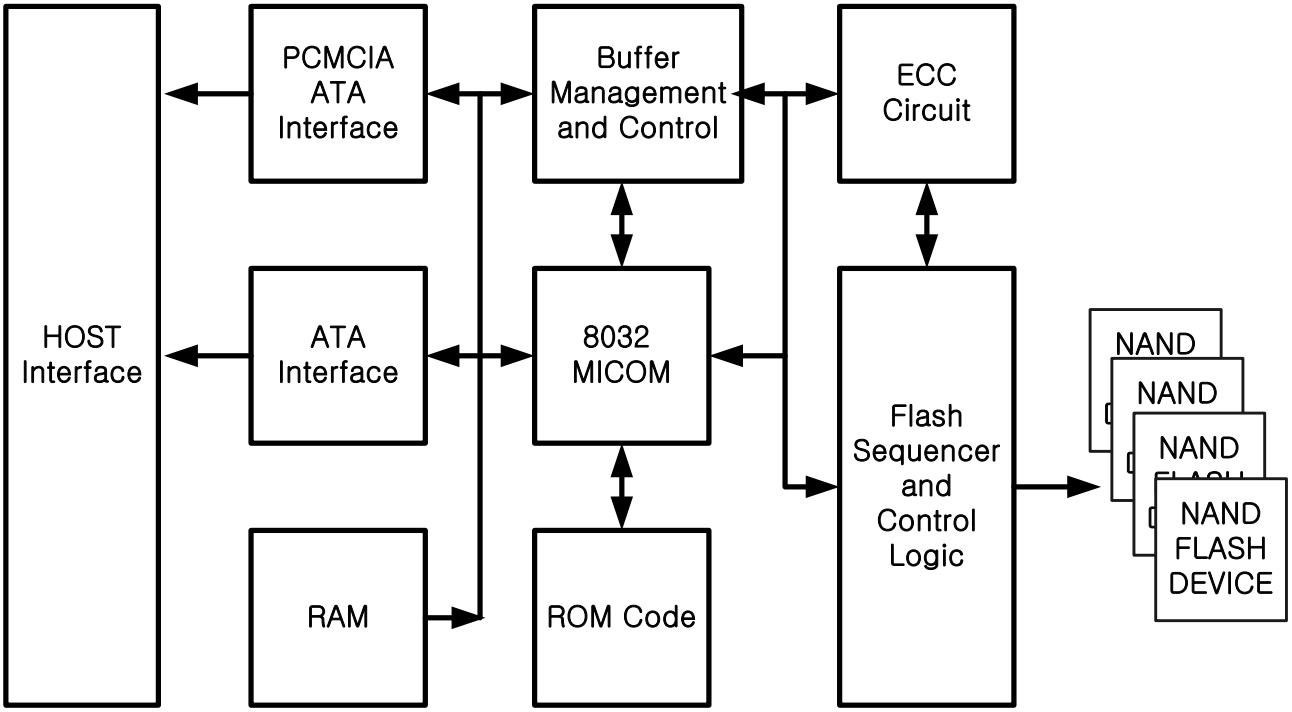


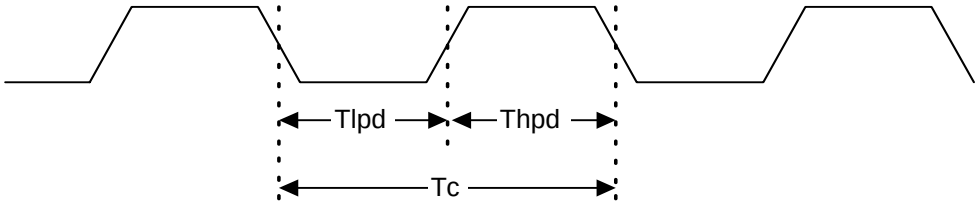
Figure 2.1 Block Diagram

3. INTERFACE BUS TIMING

ACCESS SPCIFICATIONS

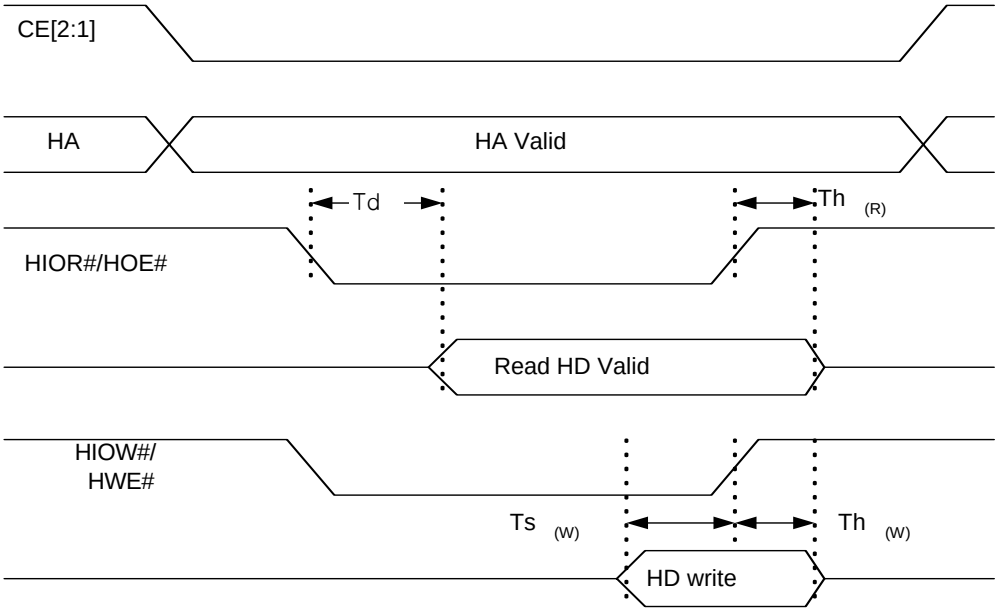
1 System clock timing

Sym.	Description	Min.	Typ.	Max.	Unit
Tc	Clock cycle time	45	50	100	ns
Tlpd	Clock low pulse duration	0.4Tc		0.6Tc	ns
Thpd	Clock high pulse duration	0.4Tc		0.6Tc	ns



2 Host Read/Write timing

Sym.	Description	Min.	Typ.	Max.	Unit
Td	HD bus asserted from HIOR# / HOE#			10	ns
$Th_{(R)}$	HD hold time after HIOR# / HOE#	40		70	ns
$Ts_{(W)}$	HD set up time of HIOW# / HWE#	10			ns
$Th_{(W)}$	HD hold time of HIOW# / HWE#	5			ns



3 Flash Read/Write timing

Sym.	Description	Min.	Typ.	Max.	Unit
$Tc_{(F)}$	Flash Read / Write cycle time		100		ns
$Ts_{(FW)}$	FD set up time of FWE#	80			ns
$Th_{(FW)}$	FD hold time of FWE#	40			ns
$Ts_{(FR)}$	FD set up time of FRD#	10			ns
$Th_{(FR)}$	FD hold time of FRD#	5			ns

REGISTERS

1) Data Register **(Address – 1F0h[170h];Offset 0,8,9)**
The Data Register is a 16-bit register, and it is used to transfer data blocks between the CompactFlash Storage Card data buffer and the Host. This register overlaps the Error Register.The table below describes the combinations of data register access and is provided to assist in understanding the overlapped Data Register and Error/Feature Register rather than to attempt to define general PCMCIA word and byte access modes and operations. See the PCMCIA PC Card Standard Release 2.0 for definitions of the Card Accessing Modes for I/O and Memory cycles.

Note: Because of the overlapped registers, access to the 1F1h, 171h or offset 1 are not defined for word (-CE2 = 0 and -CE1 = 0) operations. These accesses are treated as accesses to the Word Data Register. The duplicated registers at offsets 8, 9 and Dh have no restrictions on the operations that can be performed by the socket.

Data Register Access

DATA Register	CE2-	CE1-	A0	Offset	Data Bus
Word Data Register	0	0	X	0,8,9	D15-D0
Even Data Register	1	0	0	0,8	D7-D0
Odd Data Register	1	0	1	9	D7-D0
Odd Data Register	0	1	X	8,9	D15-D8
Error/Feature Register	1	0	1	1,Dh	D7-D0
Error/Feature Register	0	1	X	1	D15-D8
Error/Feature Register	0	0	X	Dh	D15-D8

2) Error Register (Address – 1F1h[171h];Offset 1,0Dh Read Only)
This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

Error Register

This register is also accessed on data bits D15-D8 during a write operation to offset 0 with -CE2 low and -CE1 high.
Bit 7 (BBK): this bit is set when a Bad Block is detected.
Bit 6 (UNC): this bit is set when an Uncorrectable Error is encountered.
Bit 5: this bit is 0.
Bit 4 (IDNF): the requested sector ID is not valid error or cannot be found.
Bit 3: this bit is 0.
Bit 2 (Abort) This bit is set if the command has been aborted because of a CompactFlash Storage Card status condition: (Not Ready, Write Fault, etc.) or when an invalid command has been issued.
Bit 1 This bit is 0.
Bit 0 (AMNF) This bit is set in case of a general error happened.

3) Feature Register(Address – 1F1h[171h];Offset 1,0Dh Writer Only)
This register provides information regarding features of the CompactFlash Storage Card that the host can utilize. This register is also accessed on data bits D15-D8 during a write operation to Offset 0 with -CE2 low and -CE1 high.

BIT DESCRIPTION-

7	6	5	4	3	2	1	0
Command specific							

4) Sector Count Register(Address – 1F2h[172h];Offset 2)

This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the CompactFlash Storage Card. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

BIT DESCRIPTION-

7	6	5	4	3	2	1	0
Sector Count							

5) Sector Number (LBA 7-0) Register(Address–1F3h[173h];Offset 3)
This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for any CompactFlash Storage Card data access for the subsequent command.

BIT DESCRIPTION - CHS

7	6	5	4	3	2	1	0
Sector (7: 0)							

LBA

7	6	5	4	3	2	1	0
LBA (7 : 0)							

6) Cylinder Low (LBA 15-8)Register (Address–1F4h[174h];Offset 4)
This register contains the low order 8 bits of the starting cylinder address or bits 15-8 of the Logical Block Address.

DIT DESCRIPTION-

CHS

7	6	5	4	3	2	1	0
Cylinder (7: 0)							

LBA

7	6	5	4	3	2	1	0
LBA (15 : 8)							

7) Cylinder High(LBA 23–16)Register(Address–1F5h[175h]; Offset 6)
This register contains the high order bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

BIT DESCRIPTION-

CHS

7	6	5	4	3	2	1	0
Cylinder (15 :8)							

LBA

7	6	5	4	3	2	1	0
LBA (23 : 16)							

8) Status**/**Alternate Status Register**(Address 1F7h[177h]/3F6h[376h];Offset 7/ Eh)**
These registers return the CompactFlash Storage Card status when read by the host. Reading

the Status register does clear a pending interrupt, while reading the Alternate Status register does not. The status bits are described as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

Status & Alternate Status Register

Bit 7 (BUSY): the busy bit is set when the CompactFlash Storage Card has access to the command buffer and registers and the host is locked out from accessing the command register and buffer. No other bits in this register are valid when this bit is set to a 1.
Bit 6 (DRDY): DRDY indicates whether the device is capable of performing CompactFlash Storage Card operations. This bit is cleared at power up and remains cleared until the CompactFlash Storage Card is ready to accept a command.
Bit 5 (DWF): This bit, if set, indicates a write fault has occurred.
Bit 4 (DSC): This bit is set when the CompactFlash Storage Card is ready.
Bit 3 (DRQ): The Data Request is set when the CompactFlash Storage Card requires the information to be transferred either to or from the host through the Data register.
Bit 2 (CORR): This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.
Bit 1 (IDX): This bit is always set to 0.
Bit 0 (ERR): This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error. It is recommended that media access commands (such as Read Sectors and Write Sectors) that end with an error condition should have the address of the first sector in error in the command block registers.

9) Device Control Register(Address – 3F6h[376h]; Offset Eh)
This register is used to control the CompactFlash Storage Card interrupt request and to issue an ATA soft reset to the card. This register can be written even if the device is BUSY. The bits are defined as follows:

D&	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	1	SW Rst	-IEn	0

Device Control Register

Bit 7: this bit is an X (don't care).
Bit 6: this bit is an X (don't care).
Bit 5: this bit is an X (don't care).
Bit 4: this bit is an X (don't care).
Bit 3: this bit is ignored by the CompactFlash Storage Card.
Bit 2 (SW Rst): this bit is set to 1 in order to force the CompactFlash Storage Card to perform an AT Disk controller Soft Reset operation. This does not change the PCMCIA Card Configuration Registers (4.3.2 to 4.3.5) as a hardware Reset does. The Card remains in Reset until this bit is reset to '0.'
Bit 1 (-IEn): the Interrupt Enable bit enables interrupts when the bit is 0. When the bit is 1, The interrupts from the CompactFlash Storage Card are disabled. This bit also controls the Int bit in the Configuration and Status Register. This bit is set to 0 at power on and Reset.
Bit 0: this bit is ignored by the CompactFlash Storage Card.

10) Card (Drive) Address Register(Address 3F7h[377h]; Offset Fh)
This register is provided for compatibility with the AT disk drive interface. It is recommended that this register not be mapped into the host's I/O space because of potential conflicts on Bit 7. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0

X	-WTG	-HS3	-HS2	-HS1	-HS0	-nDS1	-nDS0

Card (Drive) Address Register

Bit 7: this bit is in High Imoedence..
Implementation Note:
Conflicts may occur on the host data bus when this bit is provided by a Floppy Disk Controller operating at the same addresses as the CompactFlash Storage Card. Following are some possible solutions to this problem for the PCMCIA implementation:
1) Locate the CompactFlash Storage Card at a non-conflicting address, i.e. Secondary address (377) or in an independently decoded Address Space when a Floppy Disk Controller is located at the Primary addresses.
2) Do not install a Floppy and a CompactFlash Storage Card in the system at the same time.
3) Implement a socket adapter, which can be programmed to (conditionally) tri-state D7 of I/0 address 3F7h/377h when a Compact Flash Storage Card is installed and conversely to tri-state D6-D0 of I/O address 3F7h/377h when a floppy controller is installed.
4) Do not use the CompactFlash Storage Card's Drive Address register. This may be accomplished by either a) If possible, program the host adapter to enable only I/O addresses 1F0h-1F7h, 3F6h (or 170h-177h, 176h) to the CompactFlash Storage Card or b) if provided use an additional Primary / Secondary configuration in the CompactFlash Storage Card which does not respond to accesses to I/O locations 3F7h and 377h. With either of these implementations, the host software must not attempt to use information in the Drive Address Register.
Bit 6 (-WTG): this bit is 0 when a write operation is in progress, otherwise, it is 1.
Bit 5 (-HS3): this bit is the negation of bit 3 in the Drive/Head register.
Bit 4 (-HS2): this bit is the negation of bit 2 in the Drive/Head register.
Bit 3 (-HS1): this bit is the negation of bit 1 in the Drive/Head register.
Bit 2 (-HS0): this bit is the negation of bit 0 in the Drive/Head register.
Bit 1 (-nDS1): this bit is 0 when drive 1 is active and selected.
Bit 0 (-nDS0): this bit is 0 when the drive 0 is active and selected.

4. ATA COMMAND

CF-ATA Command Set
Table summarizes the CF-ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

Table:CF-ATA Command Set

Class	COMMAND	Code	FR	SC	SN	CY	DH	LBA
1	Check Power Mode	E5h or 98h	-	-	-	-	D	-
1	Execute Drive Diagnostic	90h	-	-	-	-	D	-
2	Format Track	50h	-	Y	-	Y	Y	Y
1	Identify Drive	ECh	-	-	-	-	D	-
1	Idle	E3h or 97h	-	Y	-	-	D	-
1	Idel Immediate	E1h or 95h	-	-	-	-	D	-
1	Initialize Drive Parameters	91h	-	Y	-	-	Y	-
1	Read Buffer	E4h	-	-	-	-	D	-
1	Read Long Sector	22h or 23h	-	-	Y	Y	Y	Y
1	Read Multiple	C4h	-	Y	Y	Y	Y	Y
1	Read Sector(s)	20h or 21h	-	Y	Y	Y	Y	Y
1	Read Verify Sector(s)	40h or 41h	-	Y	Y	Y	Y	Y
1	Recalibrate	1Xh	-	-	-	-	D	-
1	Request Sence	03h	-	-	-	-	D	-

1	Seek	7Xh	-	-	Y	Y	Y	Y
1	Set Features	EFh	Y	-	-	-	D	-
1	Set Multiple Mode	C6h	-	Y	-	-	D	-
1	Set Sleep Mode	E6h or 99h	-	-	-	-	D	-
1	Stand By	E2h or 96h	-	-	-	-	D	-
1	Stand By Immediate	E0h or 94h	-	-	-	-	D	-
1	Translate Sector	87h	-	Y	Y	Y	Y	Y
1	Wear Level	F5h	-	-	-	-	Y	-
2	Write Buffer	E8h	-	-	-	--	D	-
2	Write Long Sector	32h or 33h	-	-	Y	Y	Y	Y
3	Write Multiple	C5h	-	Y	Y	Y	Y	Y
3	WriteMultiple w/o Erase	CDh	-	Y	Y	Y	Y	Y
2	Write Sector(s)	30h or 31h	-	Y	Y	Y	Y	Y
2	Write Sector(s) w/o Erase	38h	-	Y	Y	Y	Y	Y
3	Write Verify	3Ch	-	Y	Y	Y	Y	Y

Definitions:
--**FR** = Features Register
--**SC** = Sector Count Register
--**SN** = Sector Number Register
--**CY** = Cylinder Registers
--**DH** = Card/Drive/Head Register
--**LBA** = Logical Block Address Mode Supported (see command descriptions for use).

--**Y -** The register contains a valid parameter for this command. For the Drive/Head Register Y means both the CompactFlash Storage Card and head parameters are used; D - only the CompactFlash Storage Card parameter is valid and not the head parameter.

Check Power Mode – 98h or E5h

Bit->	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Command(7)	**98h or E5h**							
C/D/H(6)	**X**			Drive	X			
Cly High(5)	**X**							
Cly Low(4)	**X**							
Sec Num(3)	**X**							
Sec Cnt(2)	**X**							
Feature(1)	**X**							

Check Power Mode

This command checks the power mode. f the CompactFlash Storage Card is in, going to, or recovering from the sleep mode, the CompactFlash Storage Card sets BSY, sets the Sector Count Register to 00h, clears BSY and generates an interrupt. If the CompactFlash Storage Card is in Idle mode, the CompactFlash Storage Card sets BSY, sets the Sector Count Register to FFh, clears BSY and generates an interrupt.

Execute Drive Diagnostic – 90h

Bit->	7	6	5	4	3	2	1	0
Command(7)	90h							
C/D/H(6)	X			Drive	X			
Cyl High(5)	X							
Cyl Low(4)	X							
Sec Num(3)	X							
Sec Cnt(2)	X							
Feature(1)	X							

Execute Drive Diagnostic

This command performs the internal diagnostic tests implemented by the CompactFlash Storage Card.
If in PCMCIA configuration this command runs only on the CompactFlash Storage Card which is addressed by the Drive/Head register when the diagnostic command is issued. This is because PCMCIA card interface does not allows for direct inter-drive communication (such as the ATA PDIAG and DASP signals). If in True IDE Mode the Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with status for both devices.
The Diagnostic codes shown in Table 39 are returned in the Error Register at the end of the command.

Diagnostic Codes

Code	ERROR TYPE
01h	No Error Detected
02h	Formatter Device Error
03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controlling Microprocessor Error
8Xh	Slave Error in True IDE Mode

Erase Sector(s) – C0h

Bit->	7	6	5	4	3	2	1	0
Command(7)	C0h							
C/D/H(6)	1	LBA	1	Drive	Head(LBA 27-24)			
Cyl High(5)	Cylinder High (LBA 23-16)							
Cyl Low(4)	Cylinder Low (LBA 15-8)							
Sec Num(3)	Sector Number (LBA 7-0)							
Sec Cnt(2)	Sector Count							
Feature(1)	X							

Erase Sector

This command is used to pre-erase and condition data sectors in advance of a Write without

Erase or Write Multiple without Erase command. There is no data transfer associated with this command but a Write Fault error status can occur.

Format Track - 50h

Bit->	7	6	5	4	3	2	1	0
Command(7)	50h							
C/D/H(6)	1	LBA	1	Drive	Head(LBA 27-24)			
Cyl High(5)	Cylinder High (LBA 23-16)							
Cyl Low(4)	Cylinder Low (LBA 15-8)							
Sec Num(3)	X (LBA 7-0)							
Sec Cnt(2)	Count (LBA mode only)							
Feature(1)	X							

Format Track

This command writes the desired head and cylinder of the selected drive with a vendor unique data pattern (typically FFh or 00h).
To remain host backward compatible, the CompactFlash Storage Card expects a sector buffer of data from the host to follow the command with the same protocol as the Write Sector(s) command although the information in the buffer is not used by the CompactFlash Storage Card.
If LBA=1 then the number of sectors to format is taken from the SecCnt register (0=256). The use of this command is not recommended.

Identify Drive - ECh

Bit->	7	6	5	4	3	2	1	0
Command(7)	ECh							
C/D/H(6)	X	X	X	Drive	X			
Cyl High(5)	X							
Cyl Low(4)	X							
Sec Num(3)	X							
Sec Cnt(2)	X							
Feature(1)	X							

Identify Drive

The Identify Drive command enables the host to receive parameter information from the CompactFlash Storage Card. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table . All reserved bits or words are zero. Table 40 is the definition for each field in the Identify Drive Information.

Table: Identify Drive Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	848Ah	2	General configuration – signature for the CompactFlash Storage Card
1	xxxxh	2	Default number of cylinders
2	0000h	2	Reserved
3	00xxh	2	Default number of heads

4	xxxxh	2	Number of unformatted bytes per track
5	xxxxh	2	Number of unformatted bytes per sector
6	xxxxh	2	Default number of sectors per track
7-8	xxxxh	4	Number of sectors per card (Word 7 = MSW , word 8 = LSW)
9	xxxxh	2	Vendor Unique
10-19	aaaa	20	Serial number in ASCII (Right Justified)
20	xxxxh	2	Buffer type
21	xxxxh	2	Buffer size in 512 byte increments
22	0004h	2	# of ECC bytes passed on Read/Write Long Commands
23-26	aaaa	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	aaaa	40	Model number in ASCII (Left Justified) Big Endian Byte Order in Word
47	xxxxh	2	Maximum number of sectors on Read/Write Mutliple command
48	0000h	2	Double Word not supported
49	xx00h	2	Capabilities
50	0000h	2	Reserved
51	0x00h	2	PIO data transfer cycle timing mode
52	0000h	2	DMA data transfer cycle timing mode
53	0001h	2	Translation parameters are valid
54	Xxxxh	2	Current numbers of cylinders
55	xxxxh	2	Current numbers of heads
56	xxxxh	2	Current sectors per track
57-58	xxxxh	4	Current capacity in sectors(LBAs)(Word 57 = LSW , Word 58 = MSW)
59	010xh	2	Multiple sector setting
60-61	xxxxh	4	Total number of sectors addressable in LBA Mode
62-127	0000h	138	Reserved
128	xxxxh	2	Security status
129-159	0000h	64	Vendor unique bytes
160	xxxxh	2	Power requirement description
161-255	0000h	170	Reserved

Idle – 97h or E3h

Bit->	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Command(7)	**97h or E3h**							
C/D/H(6)	**X**			**Drive**	**X**			

Cyl High(5)	**X**
Cyl Low(4)	**X**
Sec Num(3)	**X**
Sec Cnt(2)	**Timer Count (5 mess increments)**
Feature(1)	**X**

Idle

This command causes the CompactFlash Storage Card to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled. Note that this time base (5msec) is different from the ATA specification.

Idle Immediate – 95h or E1h

Bit->	7	6	5	4	3	2	1	0
Command(7)	**95h or E1h**							
C/D/H(6)	**X**			**Drive**	**X**			
Cyl High(5)	**X**							
Cyl Low(4)	**X**							
Sec Num(3)	**X**							
Sec Cnt(2)	**X**							
Feature(1)	**X**							

Idle Immediate

This command causes the CompactFlash Storage Card to set BSY, enter the Idle mode, clear BSY and generate an interrupt.

Initialize Drive Parameters – 91h

Bit->	7	6	5	4	3	2	1	0
Command(7)	**91h**							
C/D/H(6)	**X**	**0**	**X**	**Drive**	**Max Head(no. of heads-1)**			
Cyl High(5)	**X**							
Cyl Low(4)	**X**							
Sec Num(3)	**X**							
Sec Cnt(2)	**Number of Sectors**							
Feature(1)	**X**							

Initialize Drive Parameters

This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Card/Drive/Head registers are used by this command.

Read Buffer – E4h

Bit->	7	6	5	4	3	2	1	0
Command(7)	E4h							
C/D/H(6)	X			Drive	X			
Cyl High(5)	X							
Cyl Low(4)	X							
Sec Num(3)	X							
Sec Cnt(2)	X							
Feature(1)	X							

Read Buffer

The Read Buffer command enables the host to read the current contents of the CompactFlash Storage Card's sector buffer. This command has the same protocol as the Read Sector(s) command.

Read Multiple – C4h

Bit->	7	6	5	4	3	2	1	0
Command(7)	C4h							
C/D/H(6)	1	LBA	1	Drive	Head(LBA 27 – 24)			
Cyl High(5)	Cylinder High (LBA 23 – 16)							
Cyl Low(4)	Cylinder Low (15 – 8)							
Sec Num(3)	Sector Number (LBA 7 – 0)							
Sec Cnt(2)	Sector Count							
Feature(1)	X							

Read Multiple

The Read Multiple command performs similarly to the Read Sectors command. Interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.
Command execution is identical to the Read Sectors operation except that the number of sectors defined by a Set Multiple command are transferred without intervening interrupts. DRQ
qualification of the transfer is required only at the start of the data block, not on each sector.
The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which must be executed prior to the Read Multiple command.
When the Read Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested
sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where n = remainder (sector count / block count).
If the Read Multiple command is attempted before the Set Multiple Mode command has been executed or when Read Multiple commands are disabled, the Read Multiple operation is rejected with an Aborted Command error. Disk errors encountered during Read Multiple commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer will take place as it normally would, including transfer of corrupted data, if any Interrupts are generated when DRQ is set at the beginning of each block or partial block. The error reporting is the same as that on a Read Sector(s) Command. This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors.The transfer begins at the sector specified in the Sector Number Register.
At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command
Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer. Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block which contained the error.

Read Long Sector – 22h or 23h

Bit->	7	6	5	4	3	2	1	0
Command(7)	**22h – 23h**							
C/D/H(6)	**1**	**LBA**	**1**	**Drive**	**Head(LBA 27 – 24)**			
Cyl High(5)	**Cylinder High (LBA 23 – 16)**							
Cyl Low(4)	**Cylinder Low (15 – 8)**							
Sec Num(3)	**Sector Number (LBA 7 – 0)**							
Sec Cnt(2)	**X**							
Feature(1)	**X**							

Read Long Sector

The Read Long command performs similarly to the Read Sector(s) command except that it returns 516 bytes of data instead of 512 bytes. During a Read Long command, the CompactFlash Storage Card does not check the ECC bytes to determine if there has been a data error. Only single sector read long operations are supported. The transfer consists of 512 bytes of data transferred in word mode followed by 4 bytes of ECC data transferred in byte mode. This command has the same protocol as the Read Sector(s) command. Use of this command is not recommended.

Read Sector(s) – 20h or 21h

Bit->	7	6	5	4	3	2	1	0
Command(7)	**20h – 21h**							
C/D/H(6)	**1**	**LBA**	**1**	**Drive**	**Head(LBA 27 – 24)**			
Cyl High(5)	**Cylinder High (LBA 23 – 16)**							
Cyl Low(4)	**Cylinder Low (15 – 8)**							
Sec Num(3)	**Sector Number (LBA 7 – 0)**							
Sec Cnt(2)	**Sector Count**							
Feature(1)	**X**							

Read Sector(s)

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued and after each sector of data (except the last one) has been read by the host, the CompactFlash Storage Card sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 bytes of data from the buffer.
At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

Read Verify Sector(s) – 40h or 41h

Bit->	7	6	5	4	3	2	1	0
Command(7)	**40h – 41h**							

C/D/H(6)	1	LBA	1	Drive	Head(LBA 27 – 24)
Cyl High(5)	Cylinder High (LBA 23 – 16)				
Cyl Low(4)	Cylinder Low (15 – 8)				
Sec Num(3)	Sector Number (LBA 7 – 0)				
Sec Cnt(2)	Sector Count				
Feature(1)	X				

Read Verify Sector(s)

This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the CompactFlash Storage Card sets BSY.
When the requested sectors have been verified, the CompactFlash Storage Card clears BSY and generates an interrupt. Upon command completion, the Command Block Registers contain the cylinder, head, and sector number of the last sector verified.
If an error occurs, the verify terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

Recablibrate – 1Xh

Bit->	7	6	5	4	3	2	1	0
Command(7)	1Xh							
C/D/H(6)	1	LBA	1	Drive	X			
Cyl High(5)	X							
Cyl Low(4)	X							
Sec Num(3)	X							
Sec Cnt(2)	X							
Feature(1)	X							

Recalibrate

This command is effectively a NOP command to the CompactFlash Storage Card and is provided for compatibility purposes.

Request Sense – 03h

Bit->	7	6	5	4	3	2	1	0
Command(7)	03h							
C/D/H(6)	1	LBA	1	Drive	X			
Cyl High(5)	X							
Cyl Low(4)	X							
Sec Num(3)	X							
Sec Cnt(2)	X							
Feature(1)	X							

Request Sense

This command requests extended error information for the previous command. Table 41 defines the valid extended

error codes for the CompactFlash Storage Card Series product. The extended error code is returned to the host in the Error Register.

Extended Error Codes

Extended Error Code	Description
00h	No Error Detected
01h	Self Test OK (No Error)
09h	Miscellaneous Error
20h	Invalid Command
21h	Invalid Address (Requested Head or Sector Invalid)
2Fh	Address Overflow (address Too Large)
35h , 36h	Supply or generated Voltage Out of Tolerance
11h	Uncorrectable ECC Error
18h	Corrected ECC Error
05h , 30-34h , 37h ,3Eh	Self Test or Diagnostic Failed
10h , 14h	ID Not Found
3Ah	Spare Sectors Exhausted
1Fh	Data Transfer Error / Aborted Command
0Ch , 38h , 3Bh , 3Ch , 3Fh	Corrupted Media Format
03h	Write / Erase Failed
22h	Power Level 1 Disabled

Seek –7X h

Bit->	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Command(7)	**7Xh**							
C/D/H(6)	**1**	**LBA**	**1**	**Drive**	**Head(LBA 27 – 24)**			
Cyl High(5)	**Cylinder High (LBA 23 – 16)**							
Cyl Low(4)	**Cylinder Low (15 – 8)**							
Sec Num(3)	**X (LBA 7 – 0)**							
Sec Cnt(2)	**X**							
Feature(1)	**X**							

Seek

This command is effectively a NOP command to the CompactFlash Storage Card although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range.

Set Features - EFh

Bit->	7	6	5	4	3	2	1	0
Command(7)	EFh							
C/D/H(6)	**X**			**Drive**	**X**			
Cyl High(5)	**X**							
Cyl Low(4)	**X**							
Sec Num(3)	**X**							
Sec Cnt(2)	**Configure**							
Feature(1)	**Feature**							

Set Features

This command is used by the host to establish or select certain features. Table 45 defines all features that are supported.

Feature Supported

Feature	**Operation**
01h	Enable 8 – bit data transfers
0Ah	Enable Power Level 1 commands
55h	Disable Read Look Ahead
66h	Disable Power on Reset(POR) establishment of defaults at Soft Reset
69h	NOP – Accepted for backward compatibility
81h	Disable 8 – bit data transfer
8Ah	Disable Power Level 1 commands
96h	NOP – Accepted for backward compatibility
97h	Accepted for backward compatibility . Use of this Feature is not recommended
9Ah	Set the host current source capability. Allows tradeoff between current drawn and read/write speed.
BBh	4 bytes of data apply on Read/Write Long commands
CCh	Enable Power on Reset (POR) establishment of defaults at Soft Reset

Features 01h and 81h are used to enable and clear 8 bit data transfer modes in True IDE Mode. If the 01h feature command is issued all data transfers will occur on the low order D7D0 data bus and the IOIS16 signal will not be asserted for data register accesses.
Features 0Ah and 8Ah are used to enable and disable Power Level 1 commands. Feature 0Ah is the default feature for the CompactFlash Storage Card with extended power.
Features 55h and BBh are the default features for the CompactFlash Storage Card; thus, the host does not have to issue this command with these features unless it is necessary for compatibility reasons. Feature code 9Ah enables the host to configure the card to best meet the host system's power requirements. The host sets a value in the Sector Count register that is equal to one-fourth of the desired maximum average current (in mA) that the card should consume. For example, if the Sector Count register is set to 6, the card would be configured to provide the best possible performance without exceeding 24 mA. Upon completion of the command, the card responds to the host with the range of values supported by the card. The minimum value is set in the Cylinder Low register, and the maximum value is set in the Cylinder Hi register. The default value, after a power on reset, is to operate at the highest performance and therefore the highest current mode. The card will accept values outside this programmable range, but will operate either at the lowest power or highest performance as appropriate.
Features 66h and CCh can be used to enable and disable whether the Power On Reset (POR) Defaults will be

set when a soft reset occurs. The default setting is to revert to the POR defaults when a soft reset occurs.

Set Multiple Mode – C6h

Bit->	7	6	5	4	3	2	1	0
Command(7)	**C6h**							
C/D/H(6)	**X**			**Drive**	**X**			
Cyl High(5)	**X**							
Cyl Low(4)	**X**							
Sec Num(3)	**X**							
Sec Cnt(2)	**Sector Count**							
Feature(1)	**X**							

Set Multiple Mode

This command enables the CompactFlash Storage Card to perform Read and Write Multiple operations and establishes the block count for these commands. The Sector Count Register is loaded with the number of sectors per block. Upon receipt of the command, the CompactFlash Storage Card sets BSY to 1 and checks the Sector Count Register.
If the Sector Count Register contains a valid value and the block count is supported, the value is loaded for all subsequent Read Multiple and Write Multiple commands and execution of those commands is enabled. If a block count is not supported, an Aborted Command error is posted, and Read Multiple and Write Multiple commands are disabled. If the Sector Count Register contains 0 when the command is issued, Read and Write Multiple commands are disabled. At power on, or after a hardware or (unless disabled by a Set Feature command) software reset, the default mode is Read and Write Multiple disabled.

Set Sleep Mode – 99h or E6h

Bit->	7	6	5	4	3	2	1	0
Command(7)	**99h or E6h**							
C/D/H(6)	**X**			**Drive**	**X**			
Cyl High(5)	**X**							
Cyl Low(4)	**X**							
Sec Num(3)	**X**							
Sec Cnt(2)	**X**							
Feature(1)	**X**							

Set Sleep Mode

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timer expires so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 1.6 milliseconds. Note that this time base (1.6 msec) is different from the ATA Specification.

Standby – 96h or E2h

Bit->	7	6	5	4	3	2	1	0
Command(7)	96h or E2h							
C/D/H(6)	X			Drive	X			
Cyl High(5)	X							
Cyl Low(4)	X							
Sec Num(3)	X							
Sec Cnt(2)	X							
Feature(1)	X							

Standby

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.
Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

Standby Immediate – 94h or E0h

Bit->	7	6	5	4	3	2	1	0
Command(7)	94h or E0h							
C/D/H(6)	X			Drive	X			
Cyl High(5)	X							
Cyl Low(4)	X							
Sec Num(3)	X							
Sec Cnt(2)	X							
Feature(1)	X							

Standby Immediate

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.
Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

Translate Sector – 87h

Bit->	7	6	5	4	3	2	1	0
Command(7)	87h							
C/D/H(6)	1	LBA	1	Drive	Head(LBA 27 – 24)			
Cyl High(5)	Cylinder High (LBA 23 – 16)							
Cyl Low(4)	Cylinder Low (15 – 8)							
Sec Num(3)	Sector Number (LBA 7 – 0)							
Sec Cnt(2)	X							
Feature(1)	X							

Translate Sector

This command allows the host a method of determining the exact number of times a user sector has been erased and programmed. The controller responds with a 512 byte buffer of information containing the desired cylinder,

head and sector, including its Logical Address, and the Hot Count, if available, for that sector. Table 46 represents the information in the buffer. Please note that this command is unique to the CompactFlash Storage Card.

Address Information

ADDRESS	Information
00h – 01h	Cylinder MSB (00), Cylinder LSB (01)
02h	Head
03h	Sector
04h – 06h	LBA MSB (04) – LSB (06)
07h – 12h	Reserved
13h	Erased Flag (ffh) = Erased; 00h = Not Erased
14h – 17h	Reserved
18h – 1Ah	Hot Count MSB (18) – LSB (1A)
1bh – 1ffh	Reserved

Note 1: A value of 0 indicates Hot Count is not supported.

Wear Level – F5h

Bit->	7	6	5	4	3	2	1	0
Command(7)	**F5h**							
C/D/H(6)	**X**	**X**	**X**	**Drive**	**Flag**			
Cyl High(5)	**X**							
Cyl Low(4)	**X**							
Sec Num(3)	**X**							
Sec Cnt(2)	**Completion Status**							
Feature(1)	**X**							

Wear Level

For the CompactFlash Storage Cards that do not support security mode feature set, this command is effectively a NOP command and only implemented for backward compatibility. The Sector Count Register will always be returned with a 00h indicating Wear Level is not needed. If the CompactFlash Storage Card supports security mode feature set, this command shall be handled as Security Freeze Lock.

Write Buffer – E8h

Bit->	7	6	5	4	3	2	1	0
Command(7)	**E8h**							
C/D/H(6)	**X**			**Drive**	**X**			
Cyl High(5)	**X**							
Cyl Low(4)	**X**							
Sec Num(3)	**X**							
Sec Cnt(2)	**X**							

Feature(1)	**X**

Write Buffer

The Write Buffer command enables the host to overwrite contents of the CompactFlash Storage Card's sector buffer with any data pattern desired. This command has the same protocol as the Write Sector(s) command and transfers 512 bytes.

Write Long Sector –32h or 33h

Bit->	7	6	5	4	3	2	1	0
Command(7)	**32h or 33h**							
C/D/H(6)	**1**	**LBA**	**1**	**Drive**	**Head(LBA 27 – 24)**			
Cyl High(5)	**Cylinder High (LBA 23 – 16)**							
Cyl Low(4)	**Cylinder Low (15 – 8)**							
Sec Num(3)	**Sector Number (LBA 7 – 0)**							
Sec Cnt(2)	**X**							
Feature(1)	**X**							

Write Long Sector

This command is similar to the Write Sector(s) command except that it writes 516 bytes instead of 512 bytes. Only single sector Write Long operations are supported. The transfer consists of 512 bytes of data transferred in word mode followed by 4 bytes of ECC transferred in byte mode. Because of the unique nature of the solid-state CompactFlash Storage Card, the four bytes of ECC transferred by the host may be used by the CompactFlash Storage Card. The CompactFlash Storage Card may discard these four bytes and write the sector with valid ECC data. This command has the same protocol as the Write Sector(s) command. Use of this command is not recommended.

Write Multiple Command – C5h

Bit->	7	6	5	4	3	2	1	0
Command(7)	**C5h**							
C/D/H(6)	**X**	**LBA**	**X**	**Drive**	**Head**			
Cyl High(5)	**Cylinder High**							
Cyl Low(4)	**Cylinder Low**							
Sec Num(3)	**Sector Number**							
Sec Cnt(2)	**Sector Count**							
Feature(1)	**X**							

Write Multiple Command

Note: The current revision of the CompactFlash Storage Card only supports a block count of 1 as indicated in the Identify Drive Command information. This command is provided for compatibility with future products which may support a larger block count.

This command is similar to the Write Sectors command. The CompactFlash Storage Card sets BSY within 400 nsec of accepting the command. Interrupts are not presented on each sector but on the transfer of a block which contains the number of sectors defined by Set Multiple.

Command execution is identical to the Write Sectors operation except that the number of sectors defined by the Set Multiple command is transferred without intervening interrupts.

DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which must be executed prior to the Write Multiple command.

When the Write Multiple command is issued, the Sector Count Register contains the number of sectors (not the

number of blocks or the block count) requested. If the number of requested
sectors is not evenly divisible by the sector/block, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:
n = remainder (sector count / block count). If the Write Multiple command is attempted before the Set Multiple Mode command has been executed or when Write Multiple commands are disabled, the Write Multiple operation will be rejected with an aborted command error.
Errors encountered during Write Multiple commands are posted after the attempted writes of the block or partial block transferred. The Write command ends with the sector in error, even if it is in the middle of a block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.
The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred and the Sector Count Register contains the residual number of sectors that need to be transferred for successful completion of the command, e.g., each block has 4 sectors, a request for 8 sectors is issued and an error occurs on the third sector. The Sector Count Register contains 6 and the address is that of the third sector.

Write Multiple without Erase – CDh

Bit->	7	6	5	4	3	2	1	0
Command(7)	**CDh**							
C/D/H(6)	**X**	**LBA**	**X**	**Drive**	**Head**			
Cyl High(5)	**Cylinder High**							
Cyl Low(4)	**Cylinder Low**							
Sec Num(3)	**Sector Number**							
Sec Cnt(2)	**Sector Count**							
Feature(1)	**X**							

Write Multiple without Erase

This command is similar to the Write Multiple command with the exception that an implied erase before write operation is not performed. The sectors should be pre-erased with the Erase Sector(s) command before this command is issued.

Write Sector(s) – 30h or 31h

Bit->	7	6	5	4	3	2	1	0
Command(7)	**30h or 31h**							
C/D/H(6)	**1**	**LBA**	**1**	**Drive**	**Head(LBA 27 – 24)**			
Cyl High(5)	**Cylinder High (LBA 23 – 16)**							
Cyl Low(4)	**Cylinder Low (15 – 8)**							
Sec Num(3)	**Sector Number (LBA 7 – 0)**							
Sec Cnt(2)	**Sector Count**							
Feature(1)	**X**							

Write Sector(s)

This command writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector
Number Register. When this command is accepted, the CompactFlash Storage Card sets BSY,then sets DRQ and clears BSY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host.
For multiple sectors, after the first sector of data is in the buffer, BSY will be set and DRQ will be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It will remain in this state until the command is completed at

which time BSY is cleared and an interrupt is generated.
If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determinem what error has occurred, and on which sector.

Write Sector(s) without Erase – 38h

Bit->	7	6	5	4	3	2	1	0
Command(7)	**38h**							
C/D/H(6)	**1**	**LBA**	**1**	**Drive**	**Head(LBA 27 – 24)**			
Cyl High(5)	**Cylinder High (LBA 23 – 16)**							
Cyl Low(4)	**LBA(15 – 8)**							
Sec Num(3)	**Sector Number (LBA 7 – 0)**							
Sec Cnt(2)	**Sector Count**							
Feature(1)	**X**							

Write Sector(s) without Erase

This command is similar to the Write Sector(s) command with the exception that an implied erase before write operation is not performed. This command has the same protocol as the Write Sector(s) command. The sectors should be pre-erased with the Erase Sector(s) command before this command is issued. If the sector is not pre-erased with the Erase Sector(s) command, a normal write sector operation will occur.

Write Verify – 3Ch

Bit->	7	6	5	4	3	2	1	0
Command(7)	**3Ch**							
C/D/H(6)	**1**	**LBA**	**1**	**Drive**	**Head(LBA 27 – 24)**			
Cyl High(5)	**Cylinder High (LBA 23 – 16)**							
Cyl Low(4)	**LBA(15 – 8)**							
Sec Num(3)	**Sector Number (LBA 7 – 0)**							
Sec Cnt(2)	**Sector Count**							
Feature(1)	**X**							

Write Verify

This command is similar to the Write Sector(s) command, except each sector is verified immediately after being written. This command has the same protocol as the Write Sector(s) command.

Summaries of the valid status and error value for all the ATA Command set Error and Status Register

	Error Register					**Status Register**				
Command	BBk	UNC	IDNF	ABRT	AMNF	DRDY	DWF	DSC	CORR	ERR
CheckPowerMode					**V**	**V**	**V**	**V**		**V**
ExecuteDriveDiagnostic	**V**					**V**		**V**		**V**
Erase Sector(s)			**V**		**V**	**V**	**V**	**V**		**V**
Format Track			**V**		**V**	**V**	**V**	**V**		**V**

Identify Drive					V	V	V	V		V
Idle					V	V	V	V		V
Idle Immediate					V	V	V	V		V
InitializeDriveParameter						V		V		V
Read Buffer					V	V	V	V		V
Read Multiple	V	V	V		V	V	V	V	V	V
Read Long Sector	V		V		V	V	V	V		V
Read Sector(s)	V	V	V		V	V	V	V	V	V
Read Verify Sectors	V	V	V		V	V	V	V	V	V
Recalibrate					V	V	V	V		V
Request Sense					V	V	V	V		V
Seek			V		V	V	V			V
Set Features					V	V	V	V		V
Set Multiple Mode					V	V	V	V		V
Set Sleep Mode					V	V	V	V		V
Stand By					V	V	V	V		V
Stand By Immediate					V	V	V	V		V
Translate Sector	V		V		V	V	V			V
Wear Level	V	V	V		V	V	V	V		V
Write Buffer					V	V	V	V		V
Write Long Sector	V		V		V		V	V		V
Write Multiple	V		V		V	V	V	V		V
Write Multiple w/o Erase	V		V		V	V	V	V		V
Write Sector(s)	V		V		V	V	V	V		V
Write Sector(s) w/o Erase	V		V		V	V	V	V		V
Write Verify Sector(s)	V		V		V	V	V	V		V
Invalid Command Code					V	V	V	V		V

V = Valid on this command

Ordering Infomation

NO	Parts	Capacity	Media transfer mode	**Operation Mode**
1	DOM40S3R016	16Mbyte	BYTE	True IDE
2	DOM40S3R032	32Mbyte	BYTE	True IDE
3	DOM40S3R048	48Mbyte	BYTE	True IDE
4	DOM40S3R064	64Mbyte	BYTE	True IDE
5	DOM40S3R080	80Mbyte	BYTE	True IDE
6	DOM40S3R096	96Mbyte	BYTE	True IDE
7	DOM40S3R128	128Mbyte	BYTE	True IDE
8	DOM40S3R144	144Mbyte	BYTE	True IDE
9	DOM40S3R160	160Mbyte	BYTE	True IDE
10	DOM40S3R192	192Mbyte	BYTE	True IDE
11	DOM40S3R208	208Mbyte	BYTE	True IDE
12	DOM40S3R224	224Mbyte	BYTE	True IDE
13	DOM40S3R256	256Mbyte	BYTE	True IDE
14	DOM40S3R272	272Mbyte	BYTE	True IDE
15	DOM40S3R288	288Mbyte	BYTE	True IDE
16	DOM40S3R320	320Mbyte	BYTE	True IDE
17	DOM40S3R384	384Mbyte	BYTE	True IDE
18	DOM40S3R512	512Mbyte	BYTE	True IDE